FMA-HW01008-01 R01
Revision History

Rev	Date	Revision Description
RXX	xx-xx-xxxx	
R0A	07-30-2015	1.U11,U14,U15,U17,U18,U20,U22,U48,J2~J4,SW1~SW2,FB1~FB15,FB28,Y2,以上零件需申請新料號. 2.Y2先用EAP1024FA的XTAL暫代. 3.U39~U40暫時先用MPQ8632取代公版POWER IC的5V&1.2V電源部分,且U41~U44暫時先用MP1495取代公版POWER IC的3.3V,2.5V,1.5V&1.4V電源部分. 4.位放上去,那是用來偵測2G RF的connector,J8&J9為2P*1R的CONNECTOR,須申請料號. .J8&J9為2P*1R的CONNECTOR,須申請料號.在此頁14_BCM47452_RF,TSSI,Strap optin.
R0A	08-05-2015	BCM43217 & PoE schematic put in the schematic.
R0A	08-06-2015	1.Remove BCM47452 connection auido line. 2.格點問題已改善. 3.原U48 Power IC RT9026GQW schematic換成MP2161 schematic.
R0A	08-06-2015	ADD PoE Schematic to page 22.
R0A	08-28-2015	1.Add BCM54210E GBPHY IC schematic,Remove BCM53125 GB Switch. 2.Add PCA9535PW IC,Because the cpu need many gpio port ,it is control other interface.
R0A	08-28-2015	1.Add Diplexer schematic.
R0A	10-04-2015	1.Check 2.4G&5G schematic. 2.Add BLE schematic. 3.Add U1307 USB Switch IC in the page 7.
	10-06-2015	1.Corrct Y2, R136,U16 IO swaped
	10-20-2015	Modified parts per CE suggest.

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Model Name: BCM47452		Rev: R0B
Size: C	Page Name: 01_Revision History	Engineer: Harry Wen
Date: Friday, July 24, 2015	Sheet 1 of 24	

BCM47452 11AC

01_Revision_History
02_Tile
03_BCM47452 Block Diagram
04_Power Tree
05_BCM47452_DDR3
06_BCM47452_Flash USB 2.0
07_BCM47452_JTAG UART GPIO
08_BCM54210E_GBPHY
09_BCM54210E_Option
10_Ethernet port/LEDs
11_BCM47452_Xtal RF Power
12_BCM47452_RF,TSSI,Strap optio
13_5GHz chain 0
14_5GHz chain 1
15_BCM47452_Power/GND
16_PCIE 47452/43217
17_43217 LNA T/R SWITCH
18_43217 RF Front end
19_43217 PAs
20_43217 RF Power
21_BCM47452_Power Supplies
22_PoE TPS23754

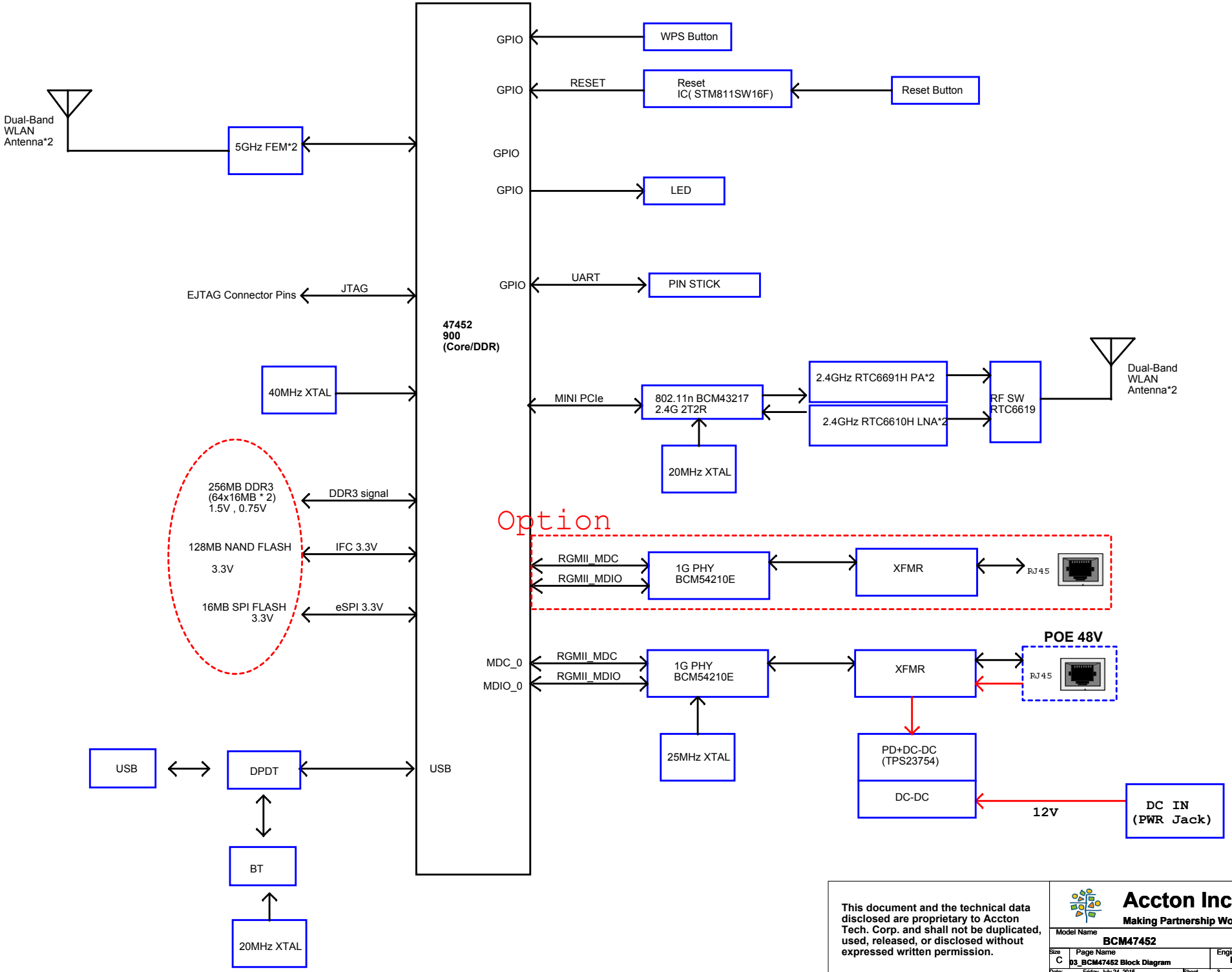
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Model Name	Rev
BCM47452	R0B

Size	Page Name	Engineer
C	02_Tile	Harry Wen

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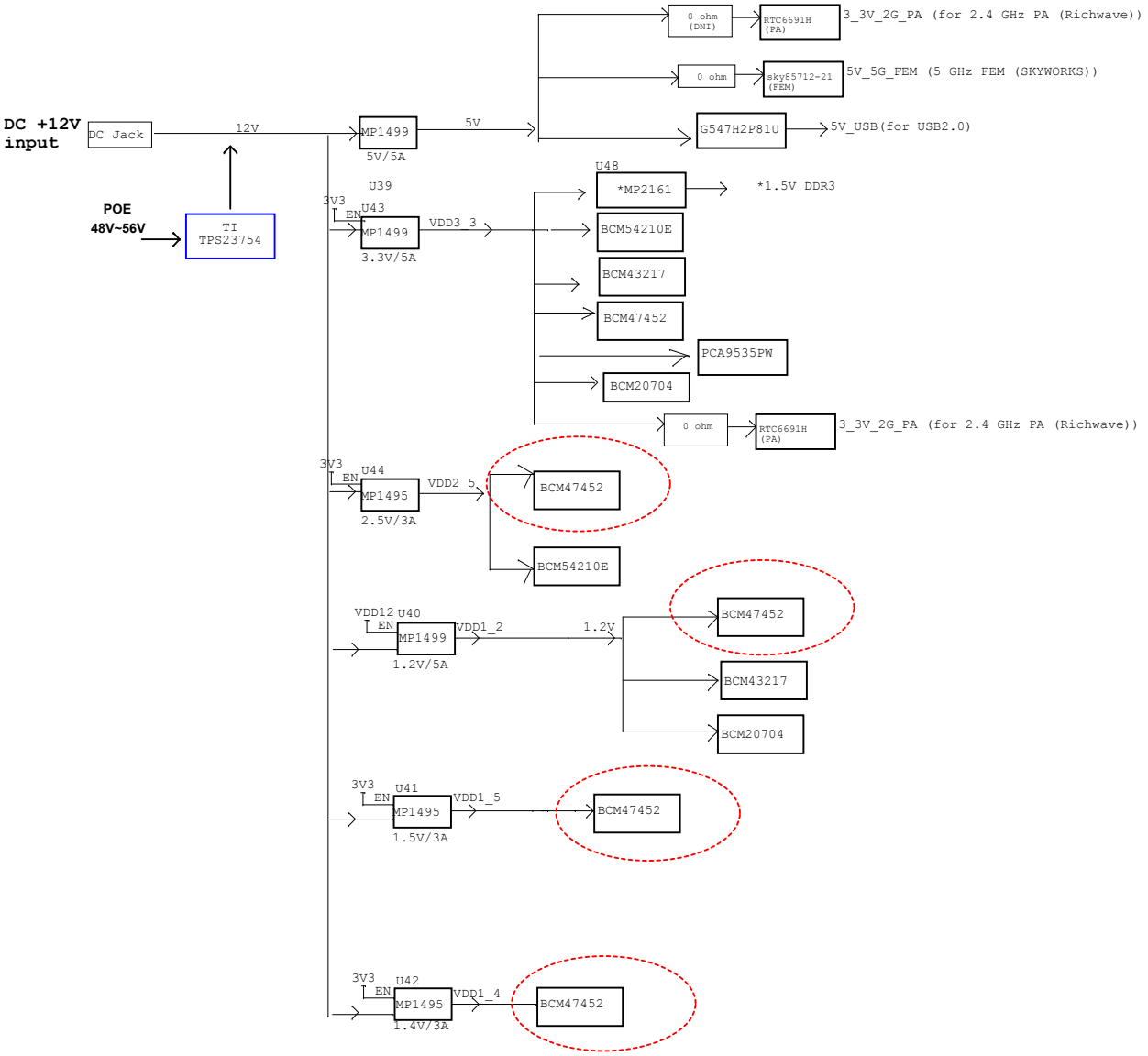
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Size	Page Name	Engineer
C	03_BCM47452 Block Diagram	Harry Wen

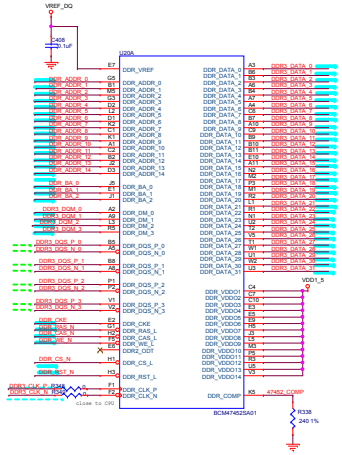
Date: Friday, July 24, 2015 Sheet 3 of 24

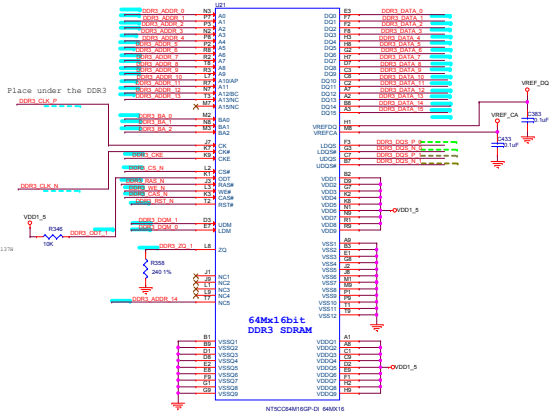


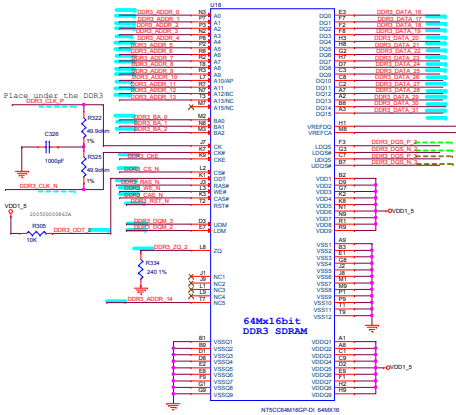
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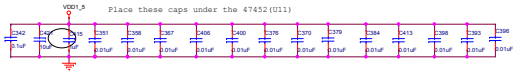
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Size D	Page Name p4_Power Tree	Engineer Harry Wen
Date: Wednesday, October 07, 2015	Sheet 4 of 24	

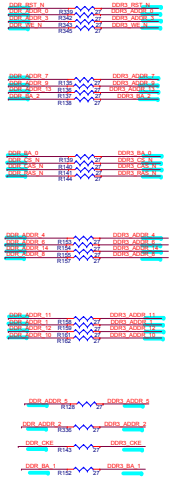




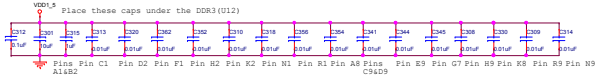


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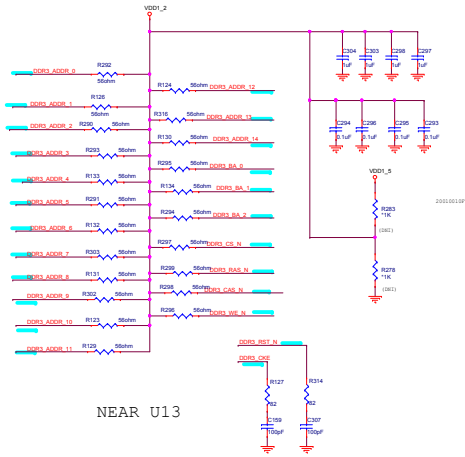




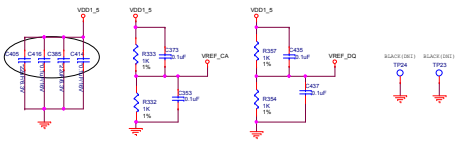
Impedance matching resistors close to 47452







NEAR U13



6 layer stackup Impedance Control Lines

100 OHM (layer#1, #6)

differential trace

W	:	5mil		
S	:	7mil	L1 ref	L2
G	:	6mil	L6 ref	L5

100 OHM (layer#3)

W	:	5mil
S	:	6.5mil
G	:	8.5mil

L3 ref L2/L4

60 OHM (layer#1, #6)

single end trace

W	:	4.5 mil
S	:	8mil

L1 ref L2
L6 ref L5

60 OHM (layer#3)

W	:	6 mil
S	:	8mil

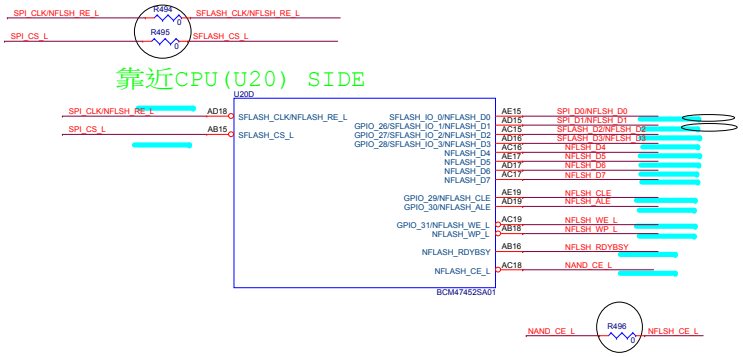
L3 ref L2/L4

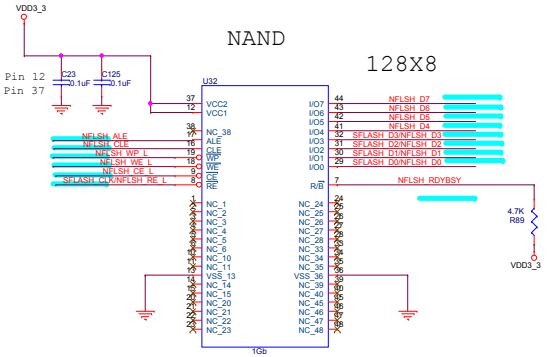
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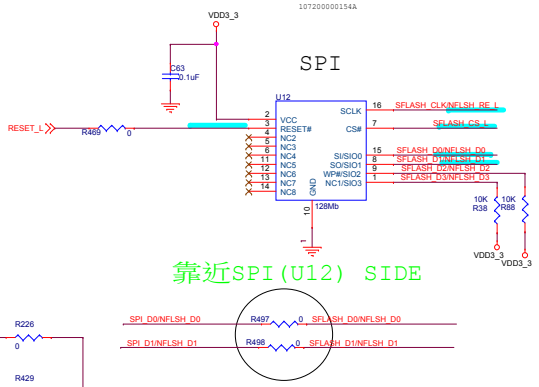
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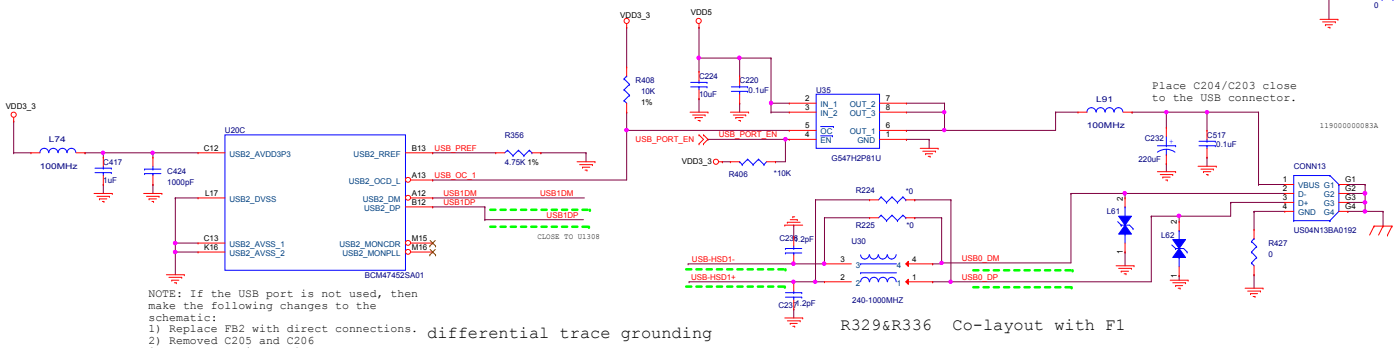
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Rev	R0B
Size	
Page Name	CustomBCM47452_DDR3
Engineer	Harry Wen
Date:	Wednesday, October 14, 2015
Sheet	5 of 24

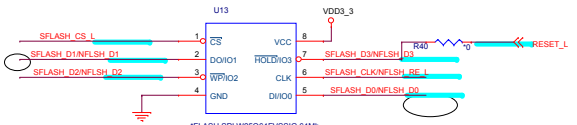
clock grounding



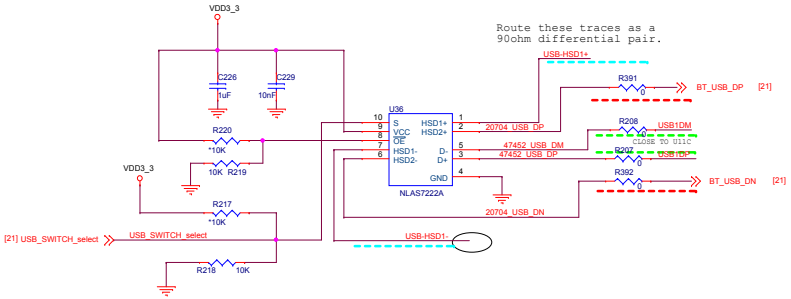








6 layer stackup Impedance Control Lines



90 OHM (layer#1, #6)

differencial trace

W	:	6mil		
S	:	6mil	L1 ref	L2
G	:	5.5mil	L6 ref	L5

100 OHM (layer#3)

W	:	7mil
S	:	6.5mil
G	:	8.5mil

L3 ref L2/L4

60 OHM (layer#1, #6)

single end trace

W	:	4.5 mil
S	:	8mil

L1 ref L2
L6 ref L5

60 OHM (layer#3)

W	:	6 mil
S	:	8mil

L3 ref L2/L4

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Size: Custom	Page Name BCM47452_Flash USB 2.0	Engineer Harry Wen
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Customer designs should use this circuit to save cost. Change the parts to "loaded".

WPS

Optional WPS functionality. Remove along with the WPS LED, if not required.

Deleted WPS key

RESET_BT
BT_WAKE

GPIO14 boot
boot GPIO17
boot GPIO18

2G

RESET BUTTON

RESET

Reset threshold = 2.93V

Optional bypass caps to supress EMI radiation from long LED traces. Place caps near the LEDs.

POWER_ACT
LAN_ACT
WLAN 2.4GHz Activity
WLAN 5GHz Activity

LED_B2B_connector

EXT LED

LAN LED PHY

WAN LED PHY

6 layer stackup Impedance Control Lines

60 OHM (layer#1, #6)

single end trace

W : 4.5 mil
S : 8mil

L1 ref L2
L6 ref L5

60 OHM (layer#3)

W : 6 mil
S : 8mil

L3 ref L2/L4

POWER LED

WAN LED

2.4G WiFi LED

5G WiFi LED

OPTION LAN LED

On Board LED

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Custom	BCM47452_JTAG UART GPIO	

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MII/GMII/RGMII - Layout Guidelines & Notes

1. Match trace lengths to a tolerance of 385 mil within TX and RX separately.
2. Keep the receive and transmit signals kept away from each other and other analog and clock signals.
3. Place capacitors and ferrite beads close to VDD traces and routes short.

6 layer stackup Impedance Control Lines

100 OHM (layer#1, #6)

differential trace

W : 5mil
S : 7mil L1 ref L2
G : 6mil L6 ref L5

100 OHM (layer#3)

W : 5mil
S : 6.5mil
G : 8.5mil

L3 ref L2/L4

60 OHM (layer#1, #6)

single end trace

W : 4.5 mil
S : 8mil

L1 ref L2
L6 ref L5

60 OHM (layer#3)

W : 6 mil
S : 8mil

L3 ref L2/L4

LAN

靠近PHY(U26) SIDE

PHY-RX

PHY-TX

CPU-TX

CPU-RX

靠近CPU(U20)SIDE

Note:
1) Both the 53125 and the 47452 have built in series terminators for a 50ohm output impedance. All RGMII traces should have a 50-60ohm impedance.
2) The TX traces, G_TXD[3:0] and G_TXCTRL, must be length matched to the G_TXC trace length to within +/-100mils. Same for RX traces relative to G_RXC.

Place C1307-C1309 physically close to DVDD pins.
Place C1310-C1312 physically close to AVDDL pins.
Place C1313-C1314 physically close to PLLVDD pins.

Place C1315-C1317 physically close to U20 AVDD pins.

When programmed for LOM LED Mode.
Then SPEED LED behavior is as below:

Speed	LED[2]	LED[1]	Status
1000BASE-T	1	0	Green(D1306 light)
100BASE-T	0	1	Green(D1307 light)
10BASE-T	1	1	off
No Link	1	1	off

LED1 0
LED2 1
LED3 0
LED4 1

TEST[3:2] = 11 for PHYA mode in which addr = 0x00 + PHYA0

54210 PHY Address

PHY Addr	TEST[3:2]	PHYA0
0x00	00	0
0x01	00	1
0x18	11	0
0x19	11	1

PHY ADDR: 0x1

BCM54210E RGMII Mode

RGMII 3.3V	00
RGMII 2.5V	01
RGMII HSTL1.5V	10
RGMII HSTL1.8V	11

Route TRD+/- pairs with 100-ohms differential trace immpedance

Board installed capacitors C1305 and C1306 values are based on a crystal specificed load capacitor, CL, value of 18 pF.
C1305 = C1306 = 2x(CL - CS)
CS = C Stray = Combined trace and pin capacitance
Place Y1301, C1305 and C1306 physically close to pins 7 and 8.
Strap the B50612E to RGMII 3.3V mode to preserve LED configuration and allow LED4 to be compatible with IRQ (open-drain with pull-up). Software configures the B50612E to the correct RGMII mode (2.5V RGMII).

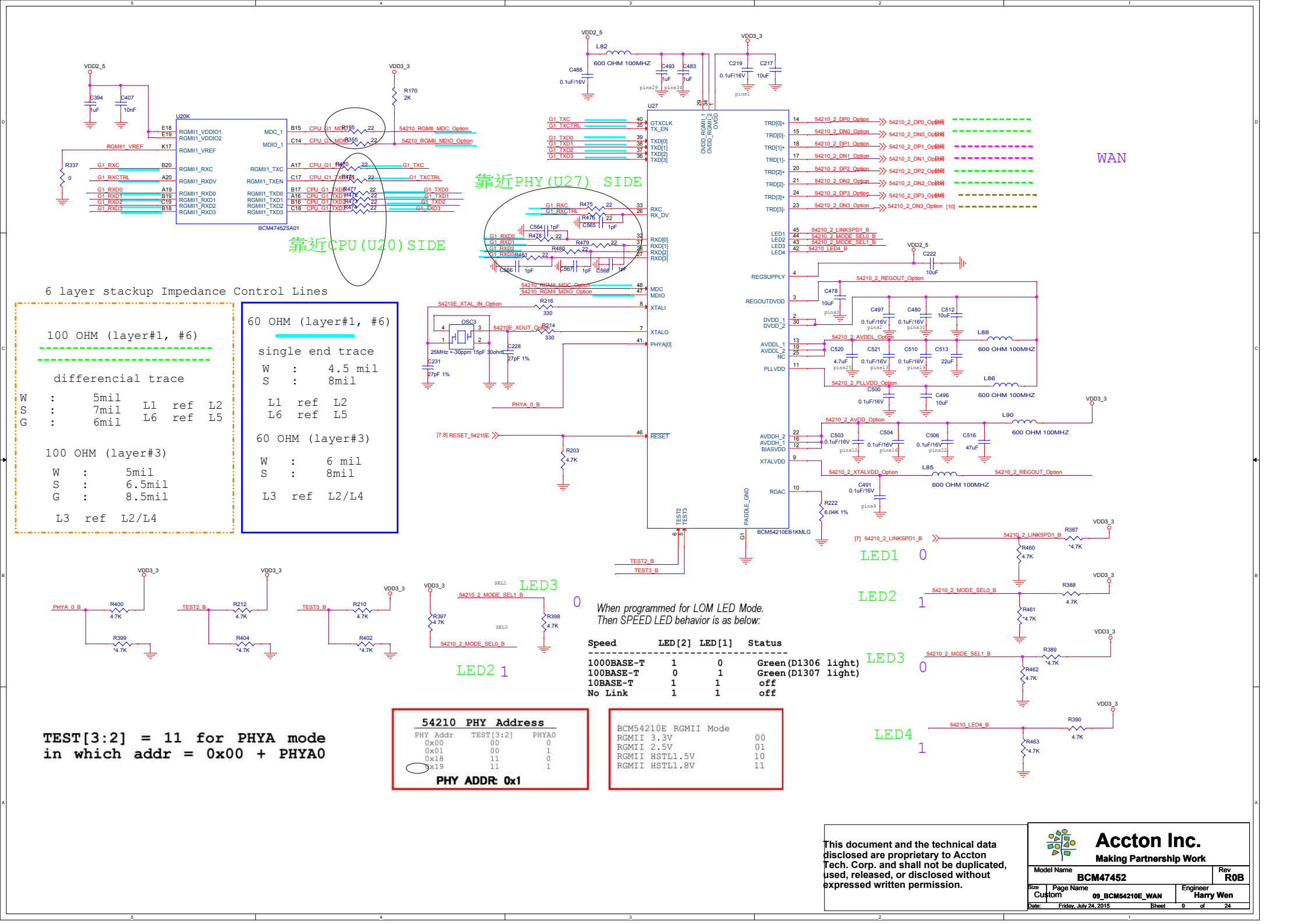
47452 RGMII strap

RGMII0_VREF	2.5V RGMII used, RGMII0_VREF =>GND 1.5V RGMII used, RGMII0_VREF =>RGMII0_VDDIO/2=0.75V	0	-
RGMII1_VREF	2.5V RGMII used, RGMII1_VREF =>GND 1.5V RGMII used, RGMII1_VREF =>RGMII1_VDDIO/2=0.75V	0	-

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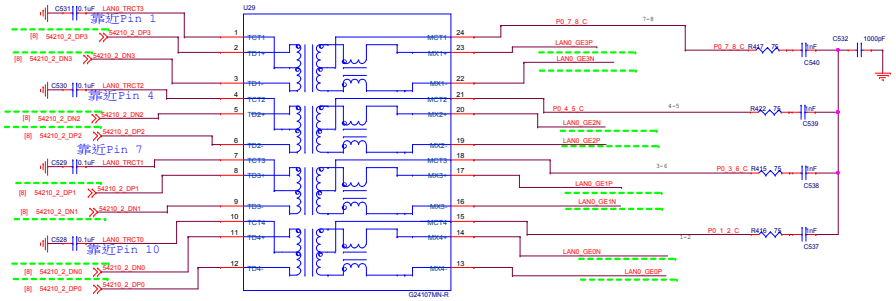
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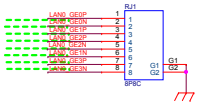
Model Name	Rev
BCM47452	R0B

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Custom	09_BCM54210E_WAN	Harry Wen

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LAN





LAN

NOTE: 100pF caps on LED signals are optional bypass caps to supress EMI radiation from long LED traces. Place caps near LEDs.

6 layer stackup Impedance Control Lines

100 OHM (layer#1, #6)

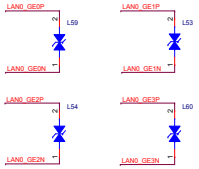
differencial trace

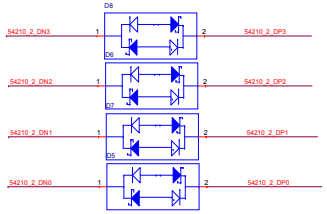
W : 5mil
S : 7mil L1 ref L2
G : 6mil L6 ref L5

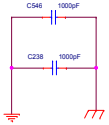
100 OHM (layer#3)

W : 5mil
S : 6.5mil
G : 8.5mil

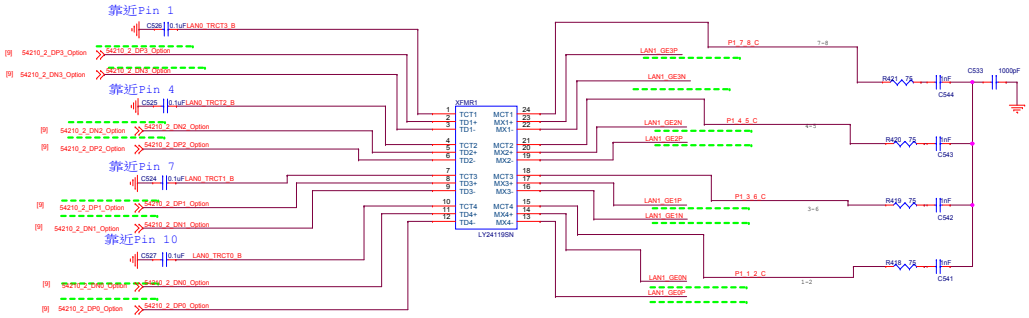
L3 ref L2/L4

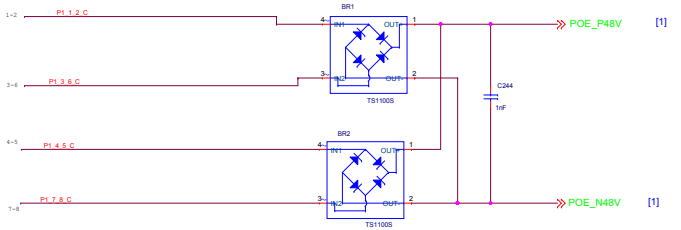


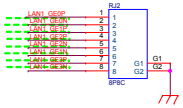




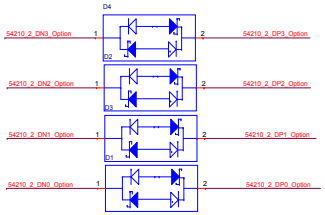
WAN

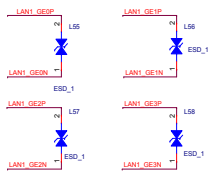


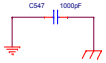




WAN







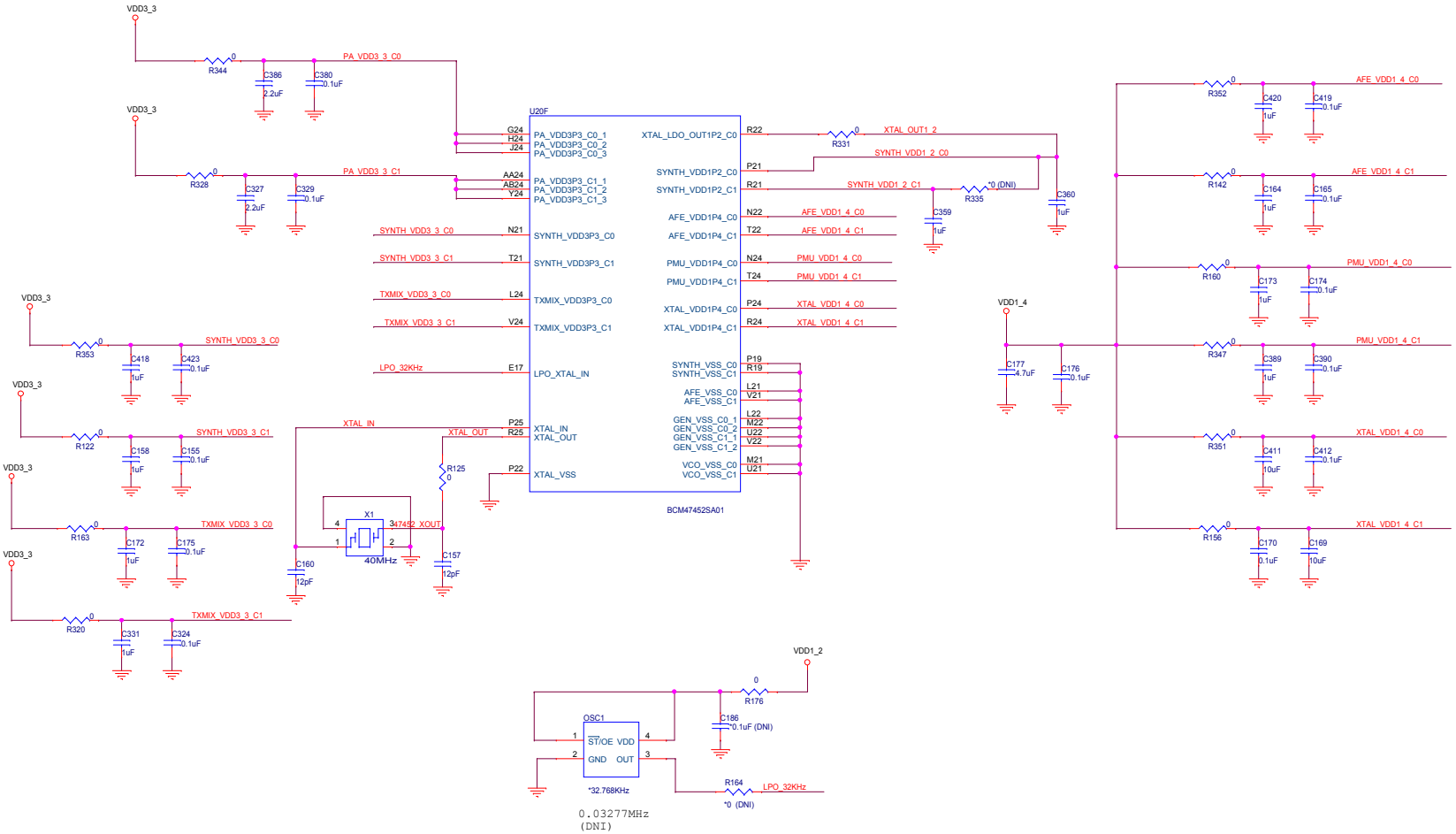
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Model Name	Rev
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Size	Page Name	Engineer
Custom	MP_Ethernet port/LEDs	Harry Won

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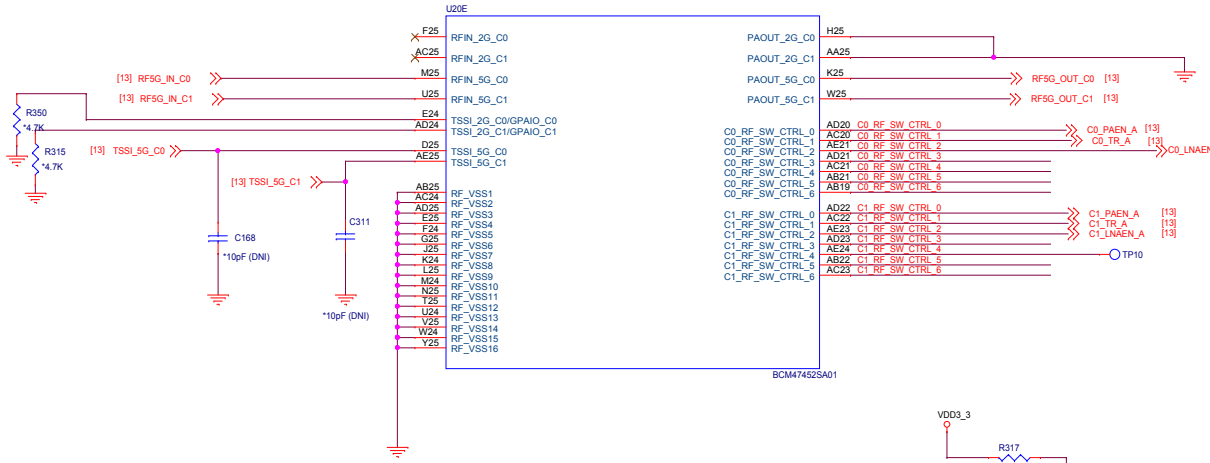
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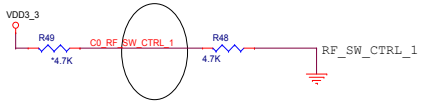
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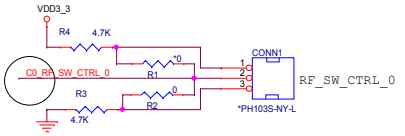
Model Name	Rev
BCM47452	R0B

Size	Page Name	Engineer
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Date: Monday, July 27, 2015 Sheet 11 of 24







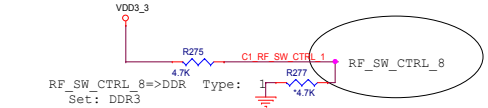
RF_SW_CTRL_[1:0]=> Boot mode: 00

Boot from Serial Flash:

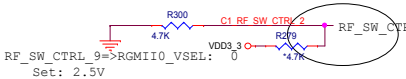
*Jumper pins 2 & 3 of J10, or leave all J10 pins open

Boot from NAND Flash:

*Jumper pins 1 & 2 of J10 to boot from NAND flash.



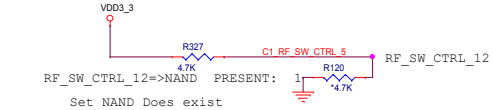
RF_SW_CTRL_8=>DDR Type: 1
Set: DDR3



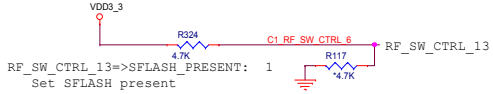
RF_SW_CTRL_9=>RGMII0_VSEL: 0
Set: 2.5V



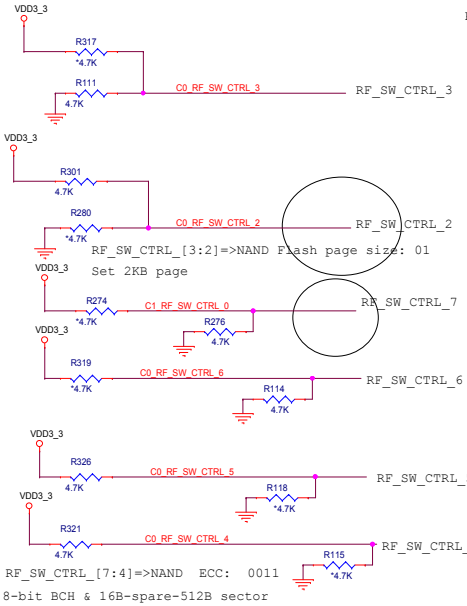
RF_SW_CTRL_10=>RGMII1_VSEL: 0
Set 2.5V

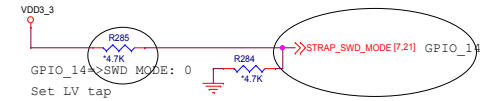


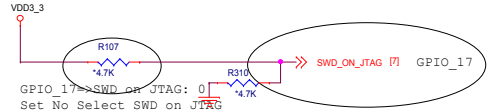
RF_SW_CTRL_12=>NAND PRESENT: 1
Set NAND Does exist

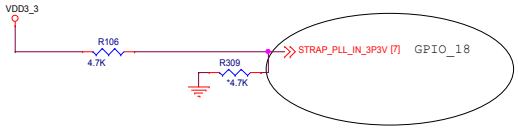


RF_SW_CTRL_13=>SFLASH_PRESENT: 1
Set SFLASH present









GPIO_18=>PLL IN 3P3V: 1

Set configure ANA_DPLLGEN40LP_M6FC in 3.3V mode

47452 Strapping option	Function	Setting	Default Pull
RF_SW_CTRL_[1:0]	Boot_Mode: 00 = Serial flash boot [default][setting] 01 = NAND boot [option] 10 = DDR boot	00	PD,PD
RF_SW_CTRL_[3:2]	NAND Flash page size: 00 = 1KB page [default] 01 = 2KB page [setting] 10 = 4KB page 11 = 8KB page	01	PD,PD
RF_SW_CTRL_[7:4]	NAND ECC: 0000 = ECC disable [default] 0001 = 1-bit Hamming (SLC) 512B sector 0010 = 4-bit BCH & 16B-spare-512B sector 0011 = 8-bit BCH & 16B-spare-512B sector [setting] 0100 = 8-bit BCH & 27B-spare-512B sector 0101 = 12-bit BCH & 27B-spare-512B sector 0110 = 24-bit BCH & 27B-spare-1K sector 0111 = 24-bit BCH & 27B-spare-1K sector 1000 = 40-bit BCH & 45B-spare-1K sector	0011	PD,PD,PD,PD
RF_SW_CTRL_8	DDR Type: 0 = DDR2 [default] 1 = DDR3 [setting]	1	PD
RF_SW_CTRL_9	RGMII0_VSEL: 0 = 2.5V [default][setting] 1 = 1.5V	0	PD
RF_SW_CTRL_10	RGMII1_VSEL: 0 = 2.5V [default][setting] 1 = 1.5V	0	PD
RF_SW_CTRL_12	NAND_PRESENT: 0 = NAND Does not exist [default] 1 = NAND Does exist [setting]	1	PD
RF_SW_CTRL_13	SFLASH_PRESENT: 0 = SFLASH not present 1 = SFLASH present [default] [setting]	1	PU
GPIO_14	SWD_MODE: 0 = LV tap [default] 1 = SWD [option]	0	PD
GPIO_17	SWD_on_JTAG: 0 = No Select SWD on JTAG [default] 1 = Select SWD on JTAG [option]	0	PD
GPIO_18	PLL_IN_3P3V: 0 = configure ANA_DPLLGEN40LP_M6FC in 1.8V mode [default] 1 = configure ANA_DPLLGEN40LP_M6FC in 3.3V mode [setting]	1	PD

* = Strapping option set at the default with no option to change.

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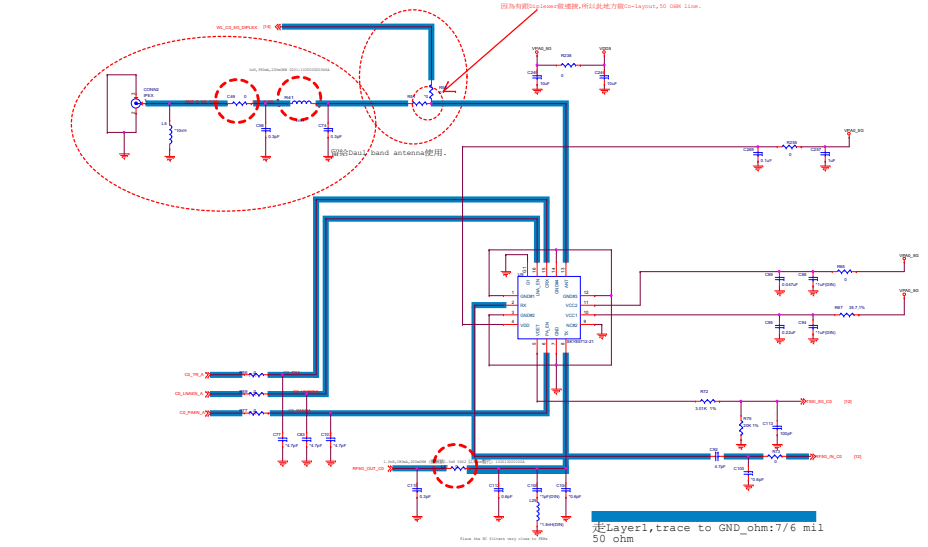
Accton Inc.

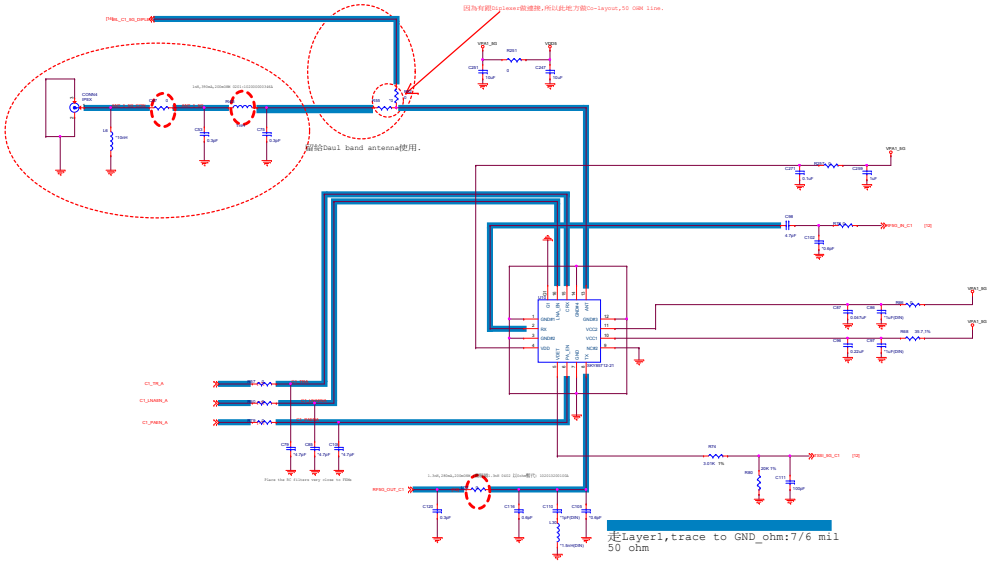
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Model Name	Rev
BCM47452	R0B

Size	Page Name	Engineer
C	12_BCM47452_RF,TSSI,Strap optio	Harry Wen

Date: Monday, July 27, 2015 Sheet 12 of 24



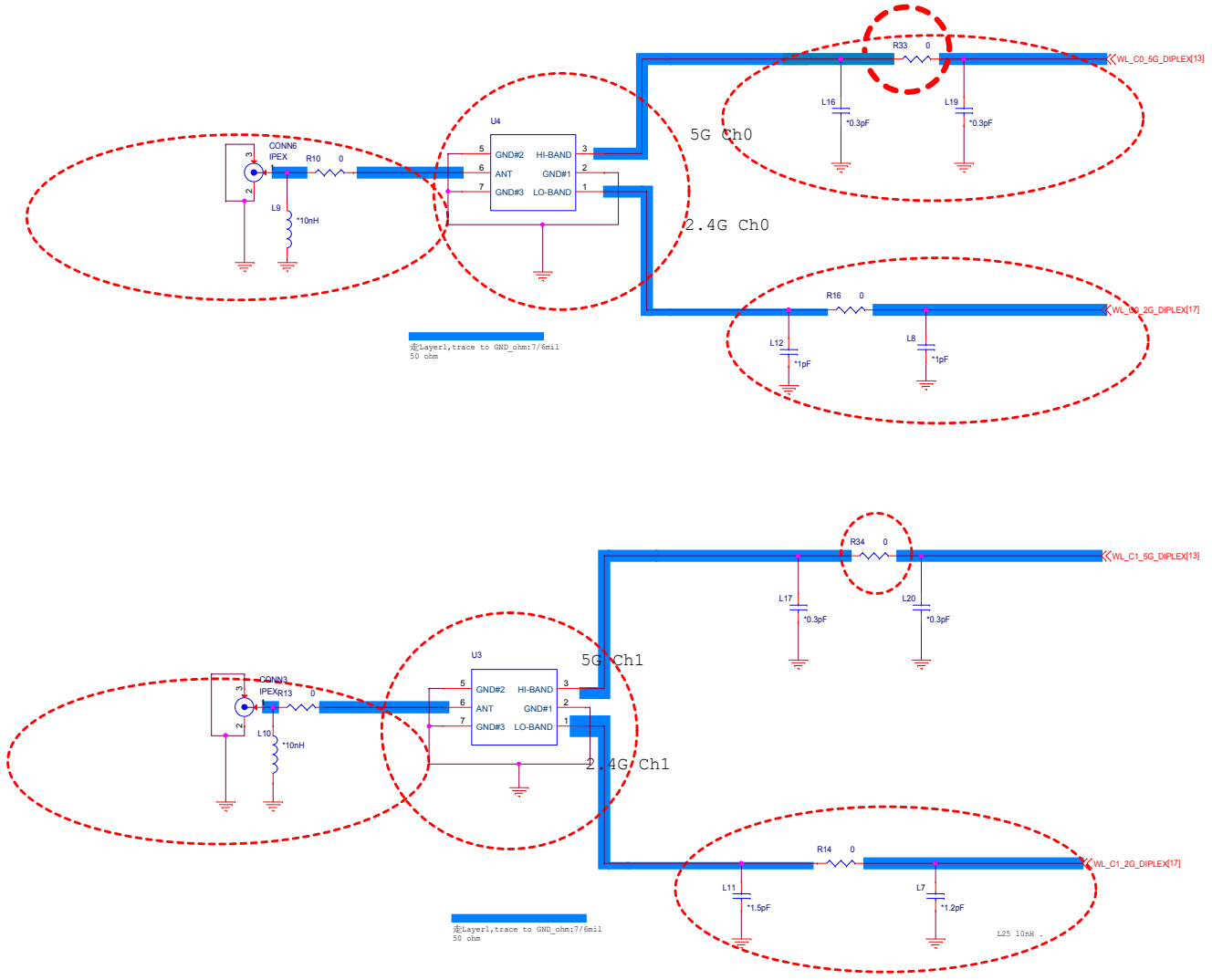


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Model Name	Rev
BCM63217	R0B
Page Name: 11_2GHz chain 0	Engineer: Michael_Shih
Size: E	Date: Wednesday, February 04, 2015

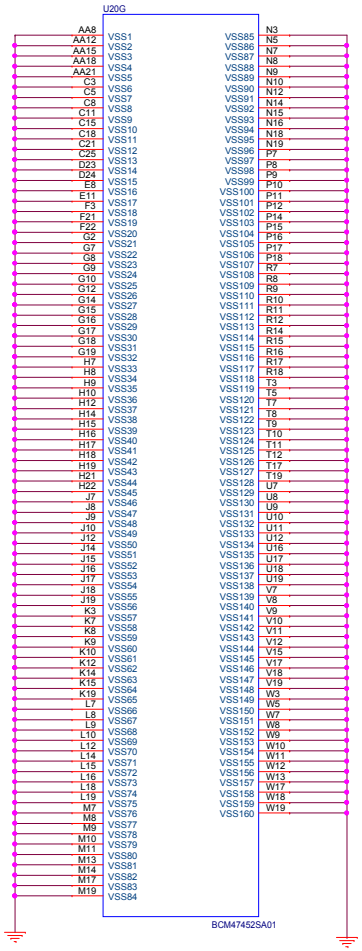
WLAN 2X2 DBDC

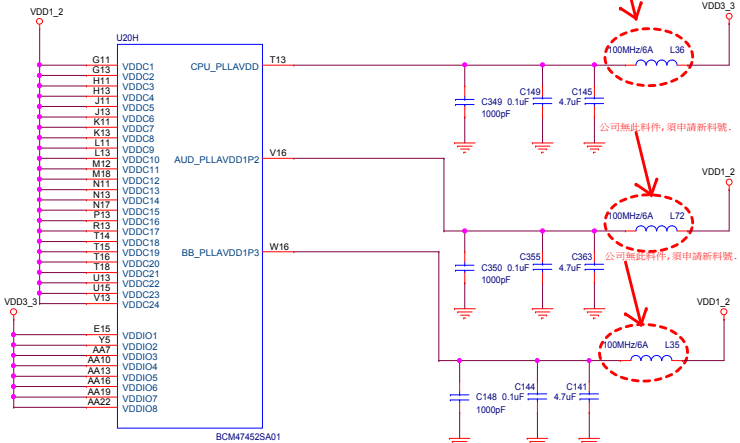


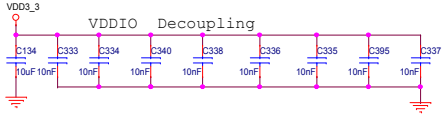
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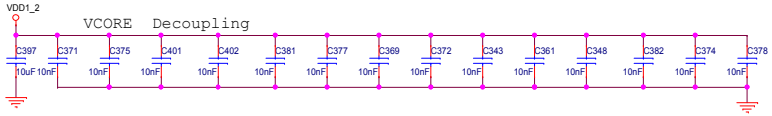
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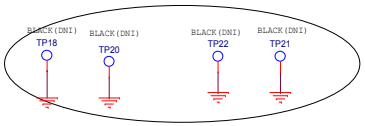
Model Name: 5GHz chain 1		Rev: R0B
Size: C	Page Name: 14_5GHz chain 1	Engineer: Michael_Shih
Date: Wednesday, February 03, 2016	Sheet 14 of 24	











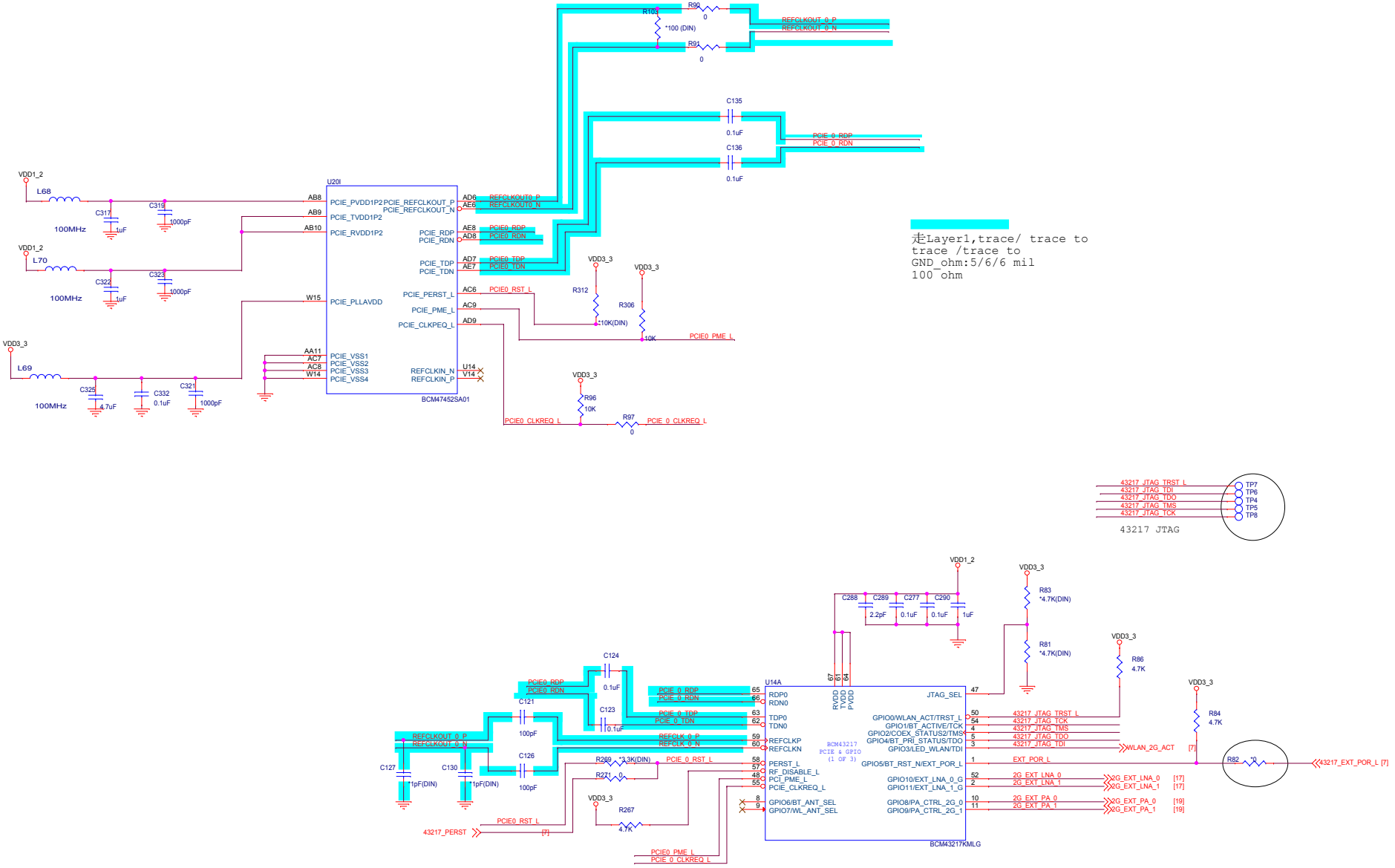
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Model Name	Rev
BCM47452	R0B

Size	Page Name	Engineer
C	15_BCM47452_Power/GND	Harry Wen

Date: Thursday, January 21, 2016 Sheet 15 of 24



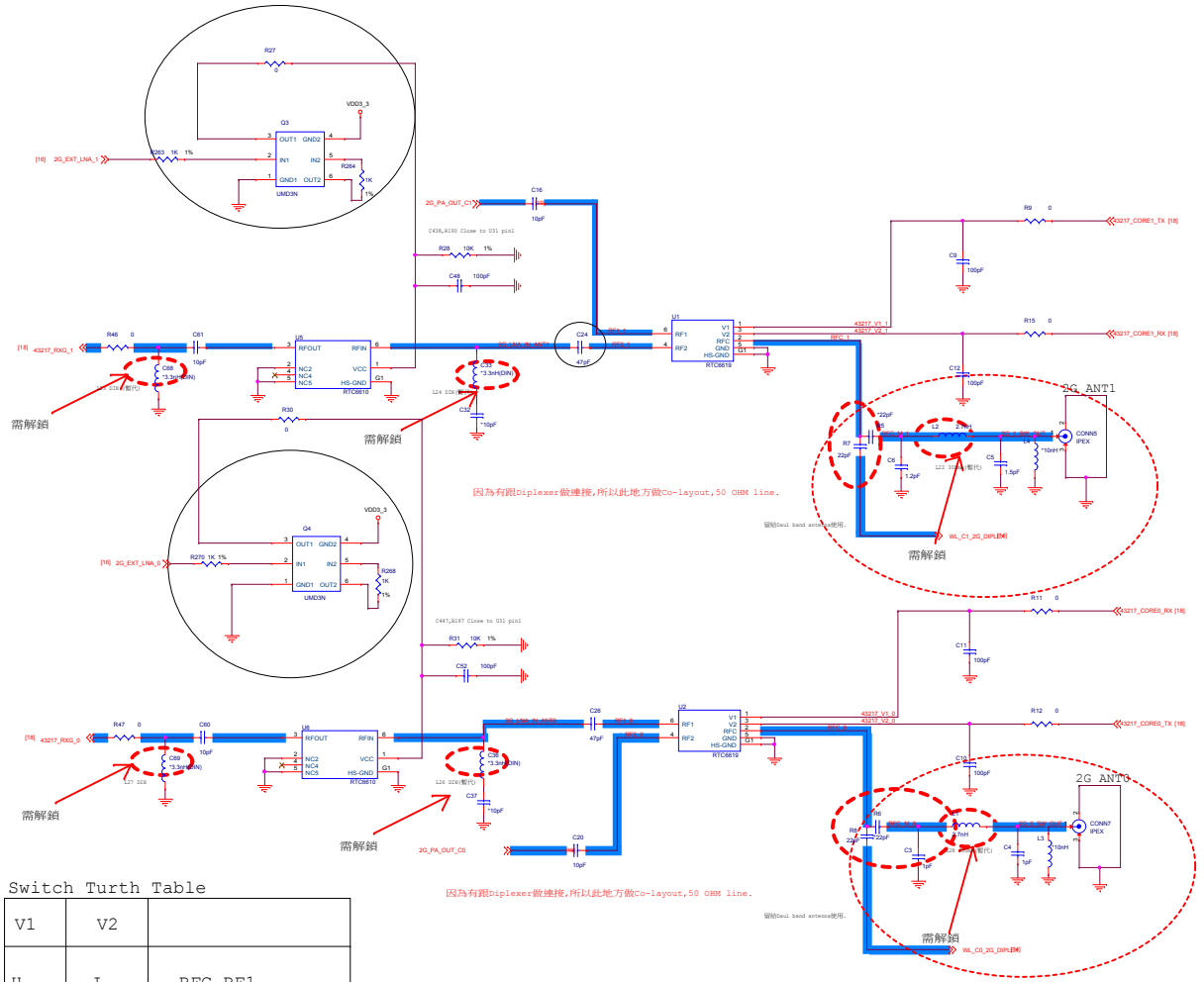
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Model Name	Rev
BCM43217	R0B

Size	Page Name	Engineer
C	16_PCIE 47452/43217	Michael_Shih

Date: Wednesday, February 03, 2016 Sheet 16 of 24



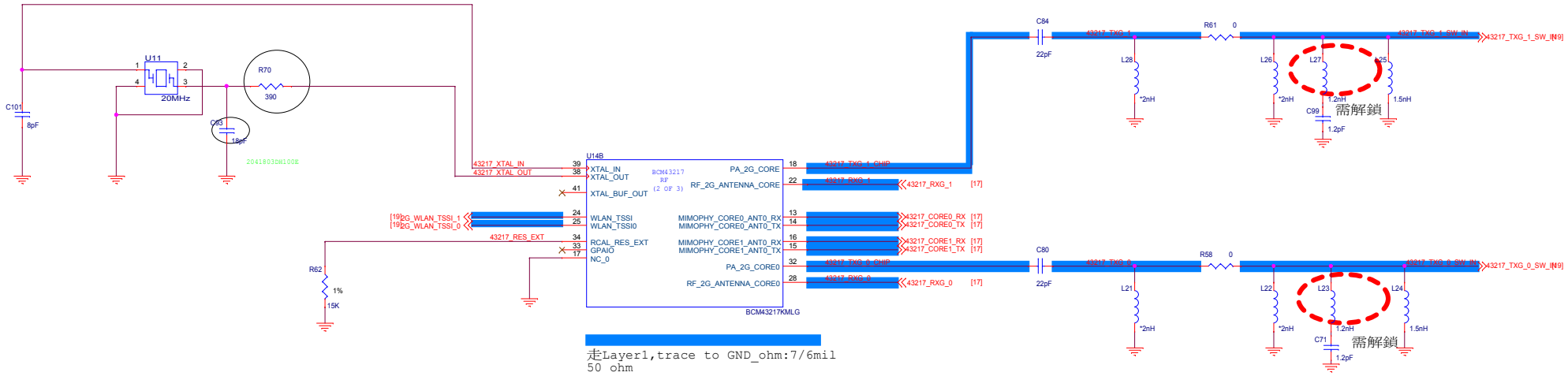
Switch Turth Table

V1	V2	
H	L	RFC-RF1
L	H	RFC-RF2

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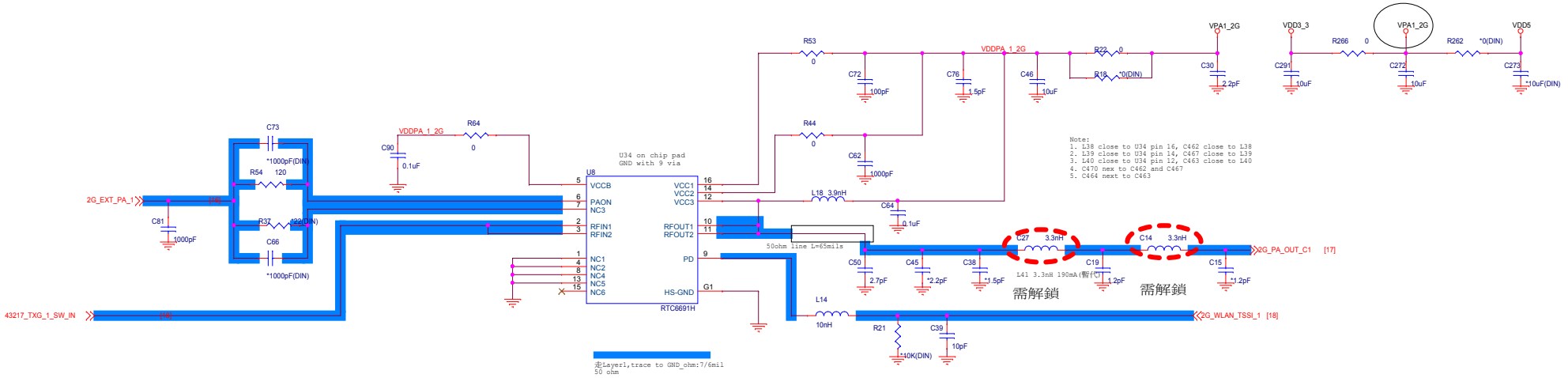
Model Name	Rev
BCM43217	R08
Size: D	Page Name: 17_43217 LNA T/R Switch
Date: Wednesday, February 03, 2016	Sheet 17 of 34
	Engineer: Michael_Shih



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Model Name: BCM43217		Rev: R0B
Size: C	Page Name: 18_43217 RF Front end	Engineer: Michael_Shih
Date: Wednesday, February 03, 2016	Sheet 18 of 24	

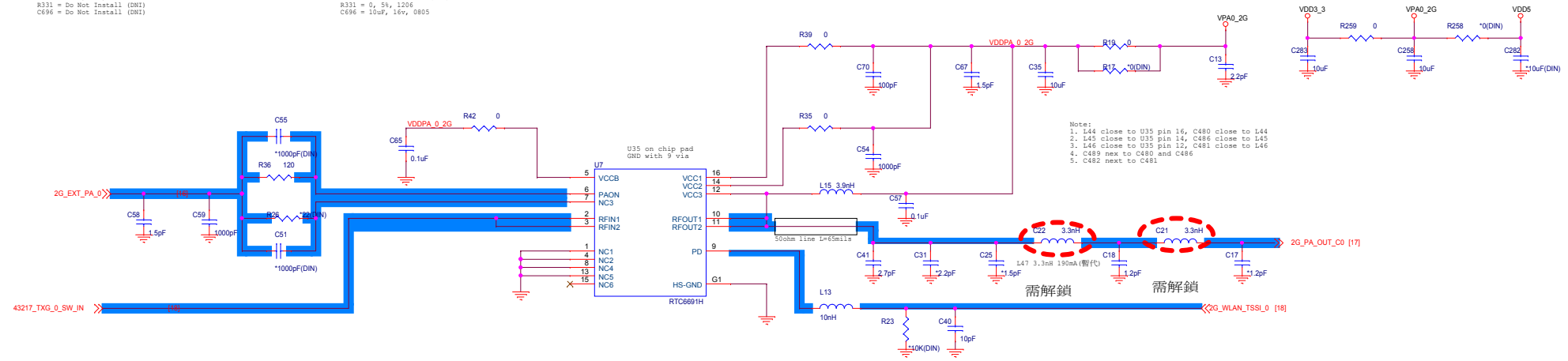


5V

Richwave RTC6649E:
U34 = Richwave RTC6649E
R211 = 22, 5%
C471 = Do Not Install (DNI)
R209 = 47, 5%
L38 = 1nH +/-0.3nH, MUATA LQG15HN1N0S02D
L39 = 3.3nH +/-0.3nH, MUATA LQG15HN3N3S02D
C472 = Do Not Install (DNI)
R212 = 10K, 1%
C473 = 2.2pF, +/-0.25pF MURATA GRM1555C1H2R2CZ01D
C474 = 1.5pF, +/-0.25pF MURATA GRM1555C1H1R5CA01D
R207 = 1, 1%, 0603
R208 = 1, 1%, 0603
R213 = 0, 5%, 1206
C479 = 10uF, 16V, 0805
R331 = Do Not Install (DNI)
C696 = Do Not Install (DNI)

3.3V

Richwave RTC6691H (Primary Choice):
U34 = Richwave RTC6691H
R211 = Do Not Install (DNI)
C471 = Do Not Install (DNI)
R209 = 0, 5%
L38 = 0, 5%
L39 = 0, 5%
C472 = 2.7pF, +/-0.25pF MURATA GRM1555C1H2R7CZ01
R212 = Do Not Install (DNI)
C473 = Do Not Install (DNI)
C474 = Do Not Install (DNI)
R207 = 0, 5%, 0603
R208 = Do Not Install (DNI)
R213 = Do Not Install (DNI)
C479 = Do Not Install (DNI)
R331 = 0, 5%, 1206
C696 = 10uF, 16v, 0805



5V

Richwave RTC6649E:
U35 = Richwave RTC6649E
R218 = 22, 5%
C490 = Do Not Install (DNI)
R216 = 47, 5%
L44 = 1nH +/-0.3nH, MUATA LQG15HN1N0S02D
L45 = 3.3nH +/-0.3nH, MUATA LQG15HN3N3S02D
C491 = Do Not Install (DNI)
R219 = 10K, 1%
C492 = 2.2pF, +/-0.25pF MURATA GRM1555C1H2R2CZ01D
C493 = 1.5pF, +/-0.25pF MURATA GRM1555C1H1R5CA01D
R214 = 1, 1%, 0603
R215 = 1, 1%, 0603
R220 = 0, 5%, 1206
C498 = 10uF, 16V, 0805
R334 = Do Not Install (DNI)
C697 = Do Not Install (DNI)

3.3V

Richwave RTC6691H (Primary Choice):
U35 = Richwave RTC6691H
R218 = Do Not Install (DNI)
C490 = Do Not Install (DNI)
R216 = 0, 5%
L44 = 0, 5%
L45 = 0, 5%
C491 = 2.7pF, +/-0.25pF MURATA GRM1555C1H2R7CZ01
R219 = Do Not Install (DNI)
C492 = Do Not Install (DNI)
C493 = Do Not Install (DNI)
R214 = 0, 5%, 0603
R215 = Do Not Install (DNI)
R220 = Do Not Install (DNI)
C498 = Do Not Install (DNI)
R334 = 0, 5%, 1206
C697 = 10uF, 16v, 0805

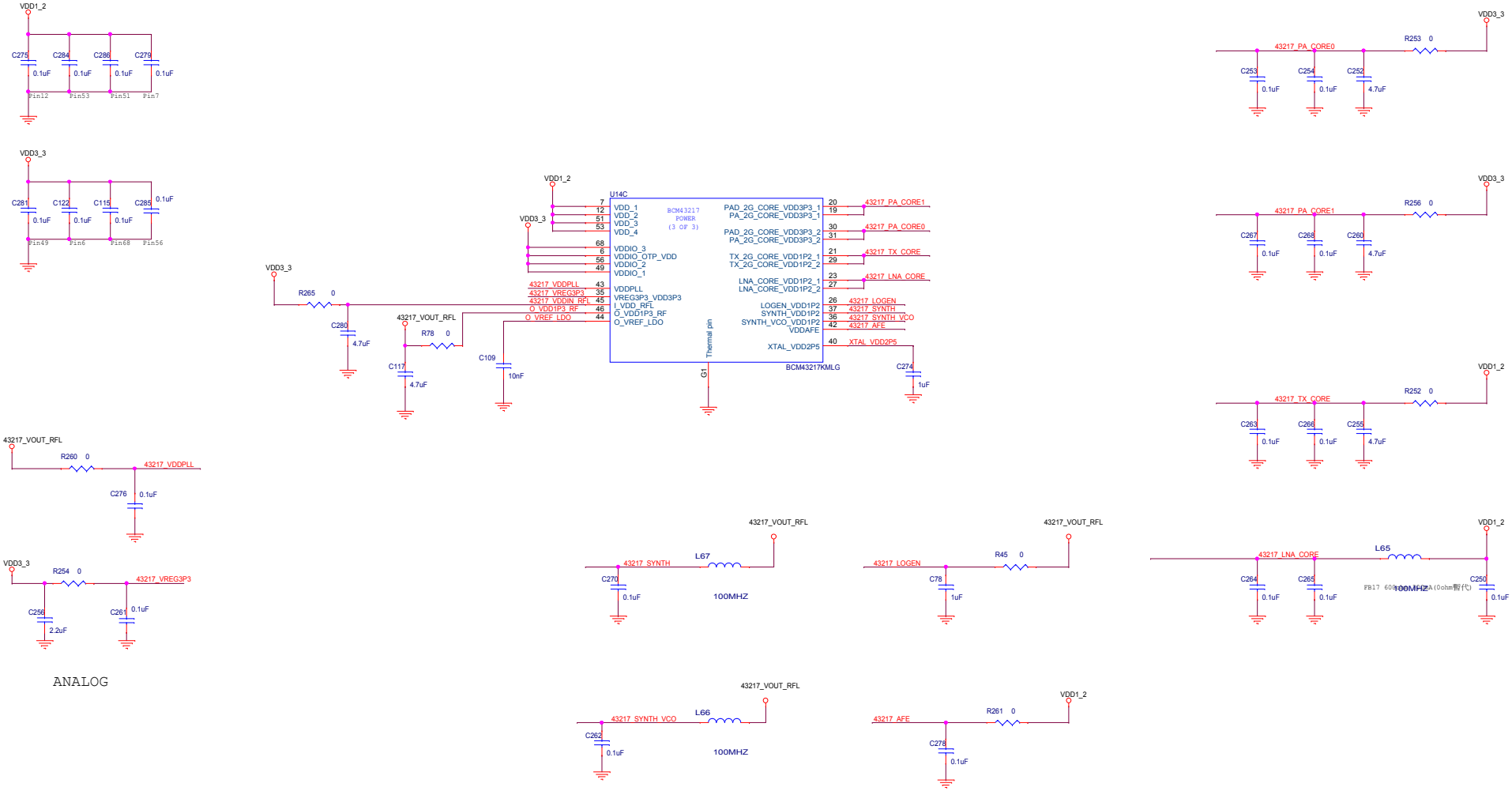
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Model Name	Rev
BCM43217	R0B

Size	Page Name	Engineer
C	19_43217 PAs	Michael_Shih

Date: Wednesday, February 03, 2016 Sheet 19 of 24



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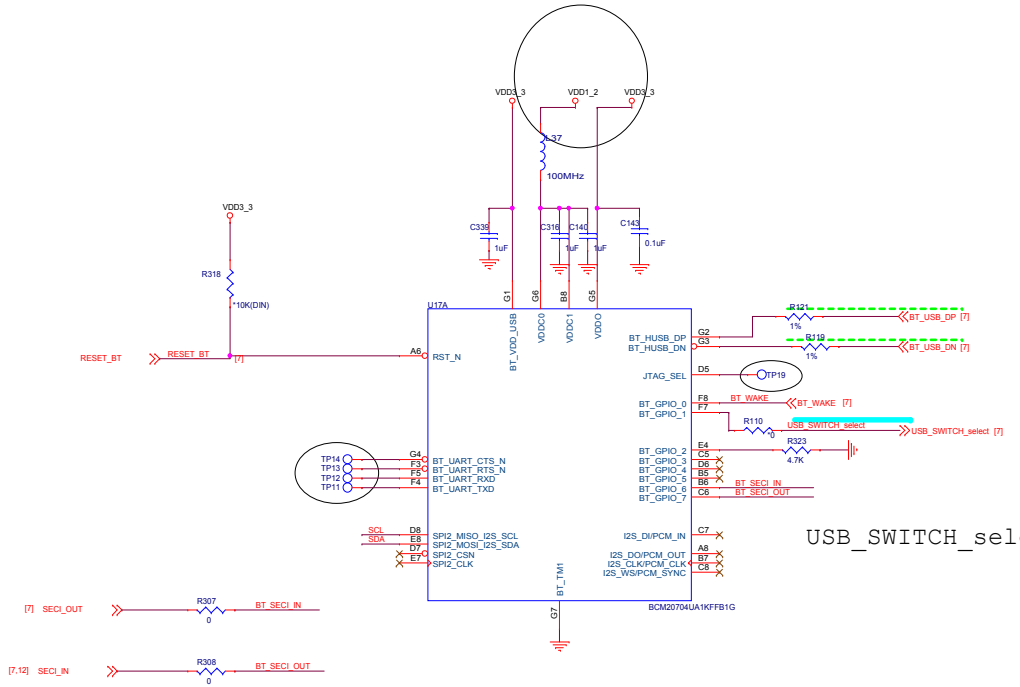
Accton

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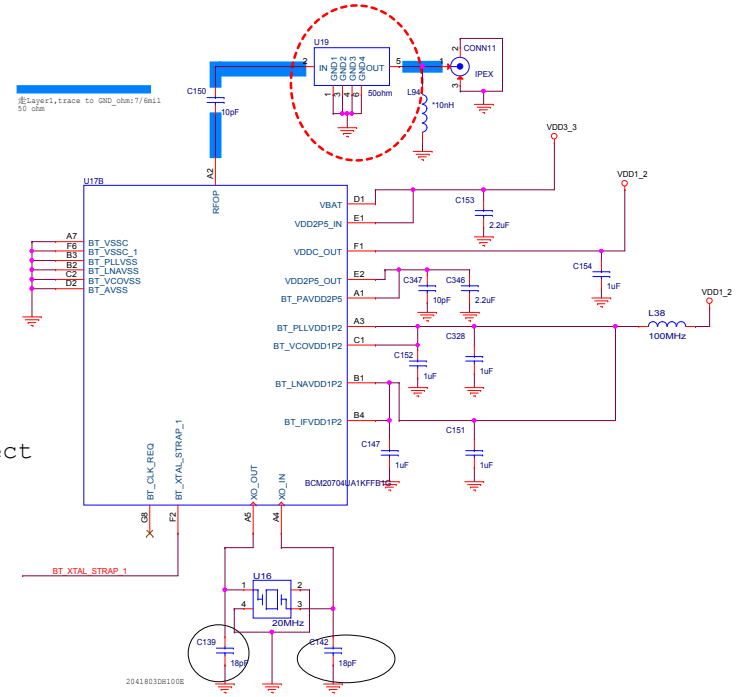
Model Name	Rev
BCM43217	R0B

Size	Page Name	Engineer
C	20_43217 RF Power	Michael_Shih

Date: Wednesday, February 03, 2016 Sheet 20 of 24



USB_SWITCH_select



6 layer stackup Impedance Control Lines

100 OHM (layer#1, #6)

differencial trace

W	:	5mil			
S	:	7mil	L1	ref	L2
G	:	6mil	L6	ref	L5

100 OHM (layer#3)

W	:	5mil
S	:	6.5mil
G	:	8.5mil

L3 ref L2/L4

60 OHM (layer#1, #6)

single end trace

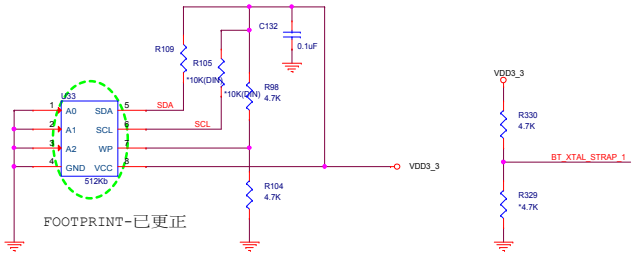
W	:	4.5 mil
S	:	8mil

L1 ref L2
L6 ref L5

60 OHM (layer#3)

W	:	6 mil
S	:	8mil

L3 ref L2/L4



FOOTPRINT-已更正

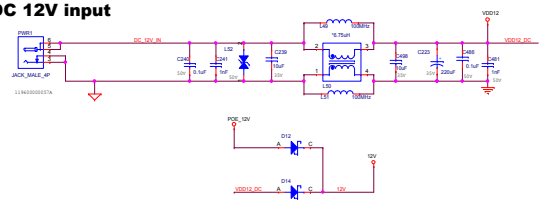
tssop_d65x5d8_8sp_3w4d41

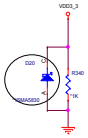
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Model Name	PoE TPS23754		Rev R0B
Size Custom	Page Name 21_BCM20704-BLE		Engineer Michael_Shih
Date: Wednesday, February 03, 2016		Sheet 21 of 24	

DC 12V input



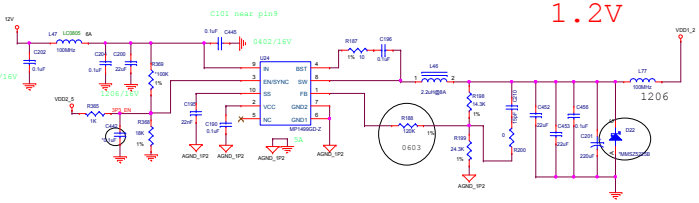


3A/5A reserved

12V ---> VDD1_2

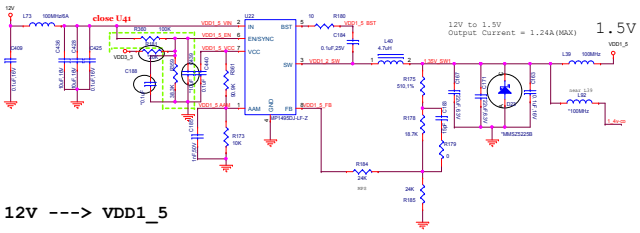
Vout =0.807*[(R1+R2) / R2]=0.807*[(14.3K+24.3K) / 24.3K]=1.28V

1.2V



12V to 1.5V

VCC5.0 = 0.807*[1+(18.7K+0.51K)/24k]=1.45V

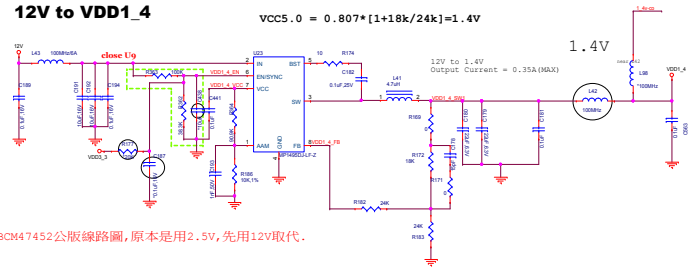


12V ---> VDD1_5

BCM47452公版線路圖,原本是用2.5V,先用12V取代.

12V to VDD1_4

VCC5.0 = 0.807*[1+18k/24k]=1.4V



BCM47452公版線路圖,原本是用2.5V,先用12V取代.

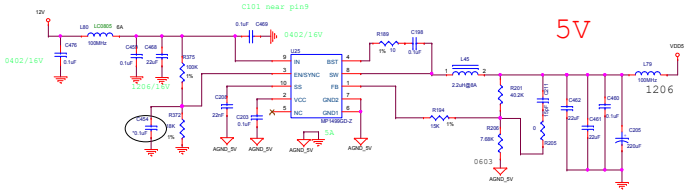
0.2USD

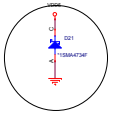
Vout =0.807*[(R1+R2) / R2]=0.807*[(40.2K+7.68K) / 7.68K]=5V

12V ---> VDD5

5A reserved

5V





200500001118H

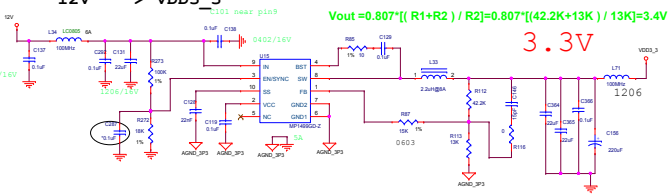
39K

12V ---> VDD3_3

5A reserved

Vout =0.807*[(R1+R2) / R2]=0.807*[(42.2K+13K) / 13K]=3.4V

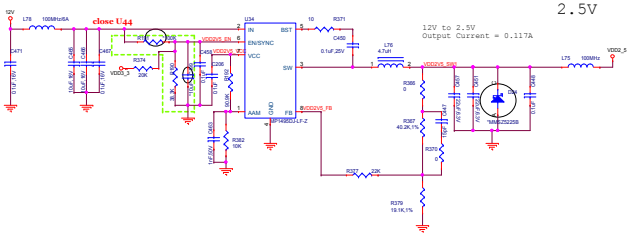
3.3V



12V ---> VDD2_5

VCC5.0 = 0.807*[1+40.2k/19.1k]=2.505V

2.5V



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Accton Inc.	Making Partnership Work
Model Name	BCM47452
Rev	R0B
Size	A
Page Name	BCM47452_Power Supplies
Engineer	
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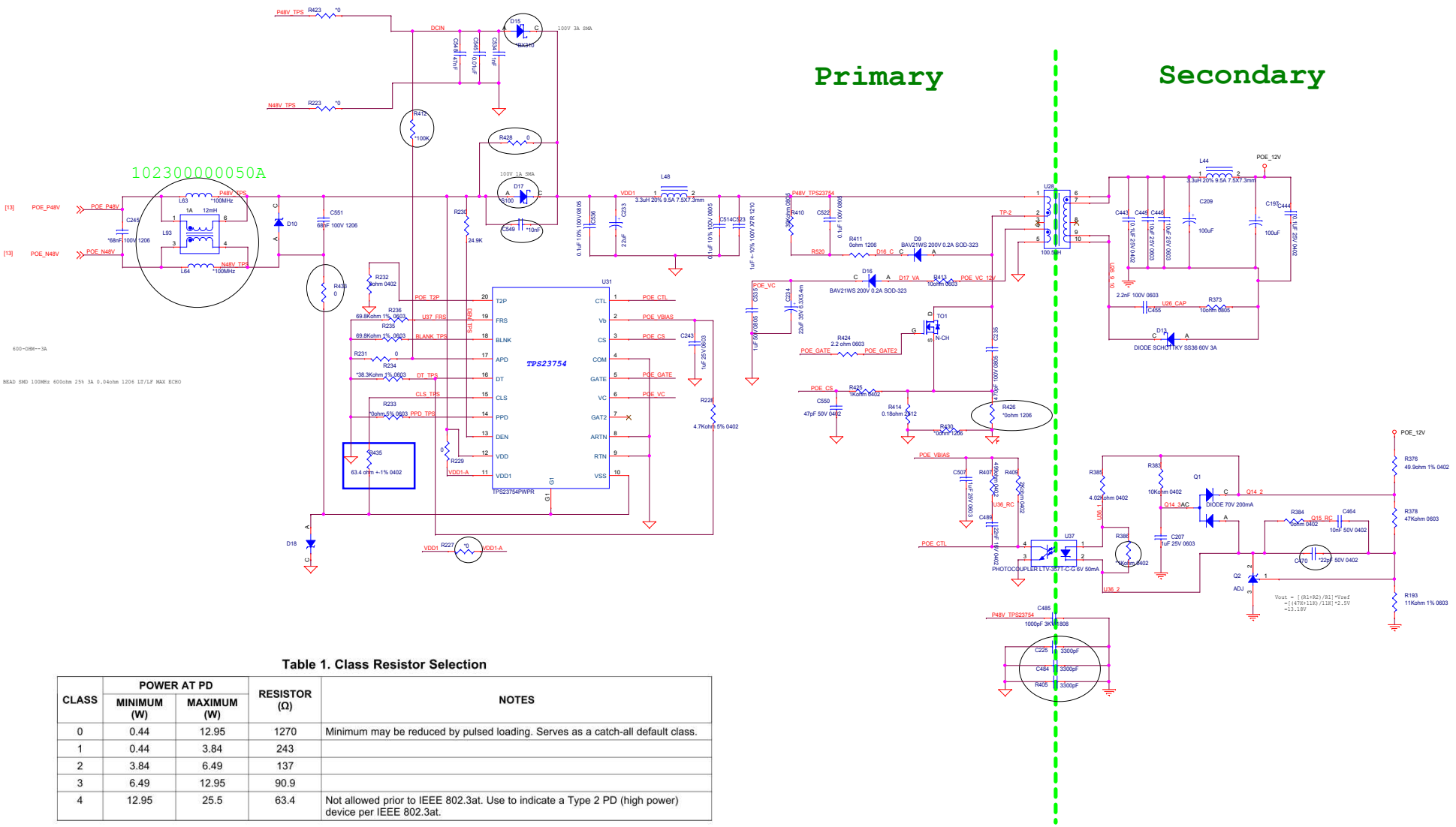


Table 1. Class Resistor Selection

CLASS	POWER AT PD		RESISTOR (Ω)	NOTES
	MINIMUM (W)	MAXIMUM (W)		
0	0.44	12.95	1270	Minimum may be reduced by pulsed loading. Serves as a catch-all default class.
1	0.44	3.84	243	
2	3.84	6.49	137	
3	6.49	12.95	90.9	
4	12.95	25.5	63.4	Not allowed prior to IEEE 802.3at. Use to indicate a Type 2 PD (high power) device per IEEE 802.3at.

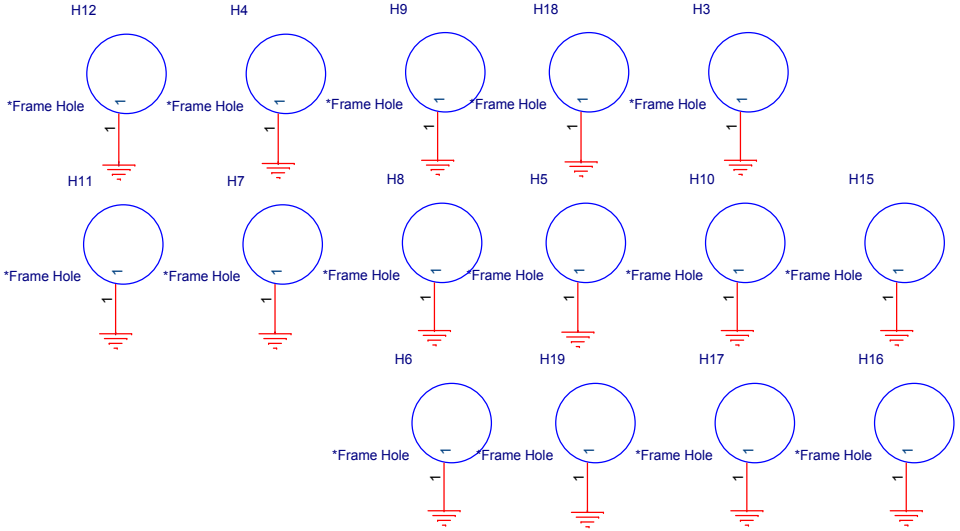
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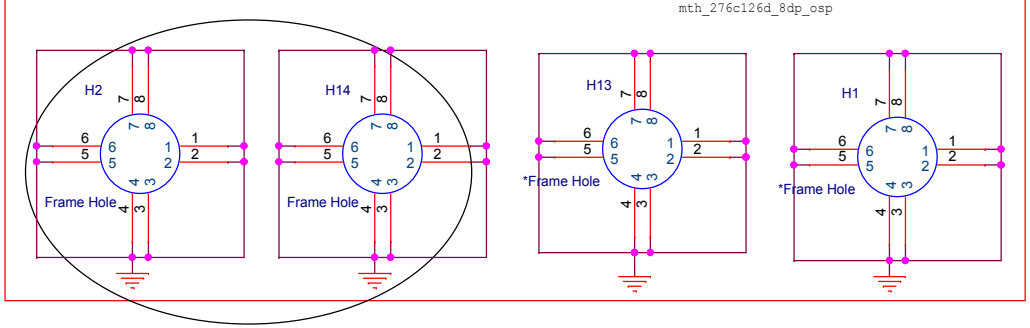
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Sheilding Holes



Enclosure Holes

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